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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,625	10/24/2001	Federico Pio	854063.512D1	1452

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EXAMINER	
KANG, DONGHEE	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,625	PIO, FEDERICO	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-15,17-21,23,24,26,29,30,32 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-14* is/are rejected.

7)☒ Claim(s) *1-3,5-8,15,17-21,23,24,26,29,30,32 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. Claims 1-3, 5-15, 17-21, 23-24, 26, 29-30, & 32-33 are pending in this application.

Claim Objections

2. Claims 1, 15,21, 26,& 30 are objected to because of the following informalities: The phrase "forming a first conductive region inside or above a substrate" is misdescriptive because the first conductive region extends above the third insulating region which is extended above the substrate (see last line in claims). The examiner suggests deleting "inside or". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsui (US 5,891,799) in view of Mochizuki et al. (US 5,990,507).

Re claim 9, Tsui teaches a method of forming an integrated semiconductor structure having a plurality of connection levels, comprising (Figs.6-11):

forming a first conductive region; forming a first insulating layer (14 & 16) having an upper surface over the first conductive region; etching a first opening through the first

insulating layer to expose a portion of the first conductive region (fig.8A); forming a first conductive plug (Fig.9) that fills the first opening and is electrically coupled to the first conductive region, the first conductive plug having an upper surface extending no further than the upper surface of the first insulating layer; forming a second insulating layer (4' & 16') having an upper surface over the first insulating layer; etching a second opening through the second insulating layer to expose a portion of the upper surface of the first conductive plug; forming a second conductive plug (20') that fills the second opening and is electrically coupled to the first conductive plug, the second conductive plug electrically contacting the upper surface of the first conductive plug, and further having an upper surface extending no further than the upper surface of the second insulating layer; forming a third opening through the first insulating layer; forming a third conductive plug that fills the third opening and has an upper surface extending no further than the upper surface of the first insulating layer, the first and third conductive plugs being formed simultaneous; forming a fourth opening through the second insulating layer; forming a fourth conductive plug that fills the fourth opening, second and fourth conductive plugs being formed simultaneous.

Tsui does not teach forming a second conductive region over the first insulating layer, the second conductive region directly coupling the third conductive plug to the fourth conductive plug. It is conventional in the art to form contact pad between two conductive plugs to prevent misalignment. Notes that Mochizuki et al. in Fig.19 teach the first wiring layer (37) formed on the first insulating films (3 & 10) and formed in such a way as to be connected to the first metal layer (35) substantially in parallel with a main

surface of the semiconductor substrate and it serves as a contact pad. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first wiring layer served as a contact pad between the first conductive plug and the second conductive plug in the Tsui's device as taught by Mochizuki in order to prevent a misalignment between the third conductive plug and the fourth conductive plug.

Re claim 10, Tsui does not explicitly teach forming the first conductive region comprises implanting a dopant into a substrate over which the first insulating layer is formed. However, Tsui noted that semiconductor device, such as FETs, are formed on the substrate and conductive layer 12 can form gate electrode for FETs (Col.4, line 65-Col.5, line 10). Therefore, it is inherent the first conductive plug is connected to source/drain regions of FETs and also Mochizuki et al. show source/drain regions.

Neither Tsui nor Mochizuki teaches ion implantation. The ion implantation is primarily used to add dopant ions into the surface of silicon wafers and has a several advantages, such as ability to more precisely control the number of implanted dopant atoms into substrate (see page 282). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use ion implantation method to form a conductive region, such as source/drain region, in a substrate of Tsui since ion implantation has ability to more precisely control the number of implanted dopant atoms into substrate to obtain a desired doping concentration.

Re claim 11, Tsui teaches the first conductive region (12) comprises depositing a semiconductor material prior to forming the first insulating layer.

Re claim 12, Tsui teaches forming the first conductive plug comprising:

Depositing a conductive layer over the first insulating layer and filling the first opening; and removing the conductive layer over the first insulating layer by polishing to leave conductive material filling the first contact via (Figs. 9-10).

Re claim 13, Tsui teaches forming the second insulating layer comprising:

Forming a first dielectric layer (4') over the first conductive region; and forming a second dielectric layer (16') over the first dielectric layer.

Re claim 14, Tsui teaches forming the second opening comprises etching through the second dielectric layer and subsequently etching through the first dielectric layer.

Allowable Subject Matter

5. Claims 1-3, 5-8, 15, 17-21, 23-24, 26, 29-30, & 32-33 would be allowable if rewritten or amended to overcome the objection, set forth in this Office action.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 571-272-1656. The examiner can normally be reached on Maxiflex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donghee Kang
Examiner
Art Unit 2811

dhk